# Evolution Based Synthesis of Analog Integrated Circuits and Systems

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#### **OUTLINE**

- Recent Trends in Electronic CAD
- Motivation
- Analog Design Automation
- Proposed Circuit-Level Synthesis System
- Results
- Extension to System Level
- Results and Conclusion

### Why Analog Design Automation

- Design automation very successful in digital domain
- Most designs moving towards SOC
- Analog sections required for most applications
- Digital design covers 90% of area
- 90% of effort spent on analog design



Knowledge-based and Optimization-based Analog Circuit Design Automation

# Circuit Level Analog Synthesis

- Given a circuit topology, find transistor channel
  W/L ratios and reference (bias) voltages to attain desired performance such as gain, bandwidth etc.
- A difficult constrained optimization problem
- Many different approaches present in the literature
- Our approach will be presented here

## Circuit Level Analog Synthesis

- Our approach consists of the following:
  - A constrained optimization to which cii®uit synthesis problem is mapped
  - A novel high performance search algorithm based on combining Evolution Strategies & Simulated Annealing
  - A fast de circuit simulator
  - User defined equations and neural performance models for ac behavior
  - Incorporation of real life IC parameter variations

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# Circuit Level Analog Synthesis

• Problem representation (search variables of the optimizer) as chromosome encoding:

$$X_{x} = [W_{1}, ..., W_{t}, L_{1}, ..., L_{t}, B_{1}, ..., B_{k}]$$

• Generation of candidate solutions via ES

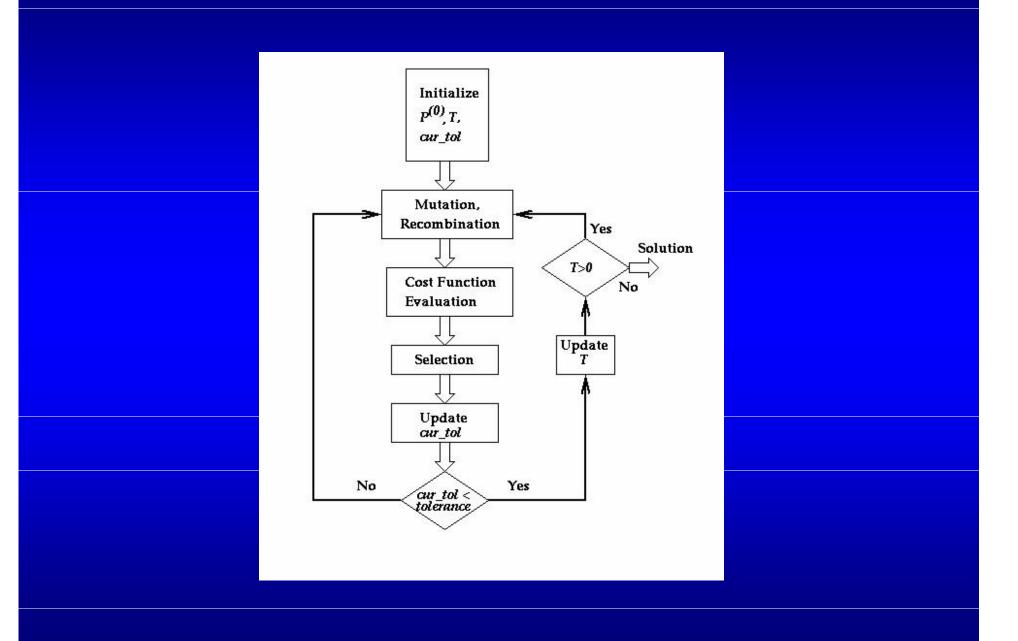
• Minimization of cost function C(x):

$$C(x) = \sum w_i f_i(x) + \sum w_i g_i(x)$$

(requires evaluation in each pass)

# Why new optimizer?

- Current optimization tools not that successful in complex problems
- ES finds the correct solution region, but cannot converge easily to specific solutions
- SA converges to correct solution, but cannot find correct region easily
- Our approach combines these two and is demonstrated to be superior to both for many examples



# Why dc simulator

- Many people use symbolic analysis for dc solution
- Symbolic analysis faster, but approximate
- All performance parameters depend on dc solution
- If symbolic analysis is used, simulation must be done every 5-10 steps to verify results
- Our approach is comparable in speed, but more accurate

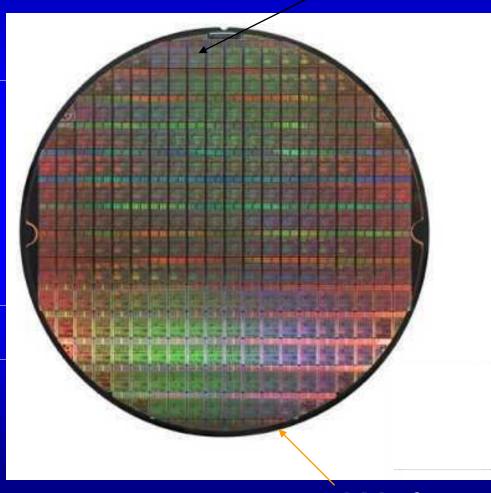
# Why ac performance models

- AC performance parameters (gain, BW, etc) can be calculated to a high accuracy using small signal models
- User can derive equations => very fast evaluation
- Neuro-fuzzy performance models => automatic generation of models possible
- Flexibility between equations and NNs

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#### Variation Tolerance

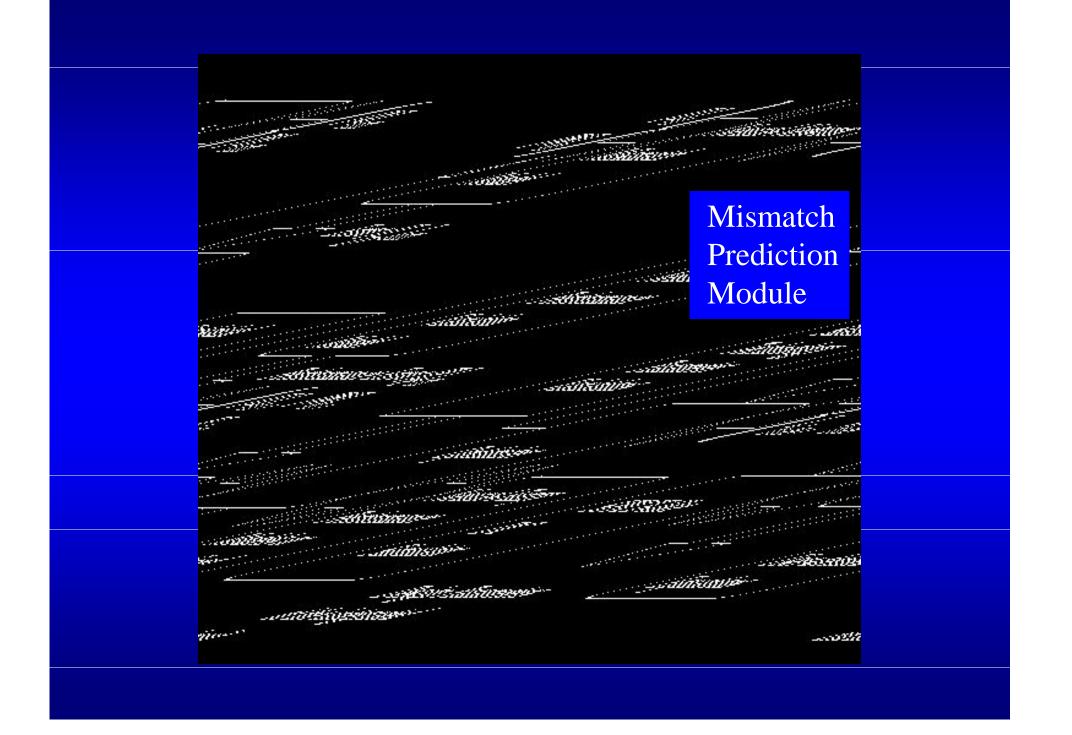
Single die

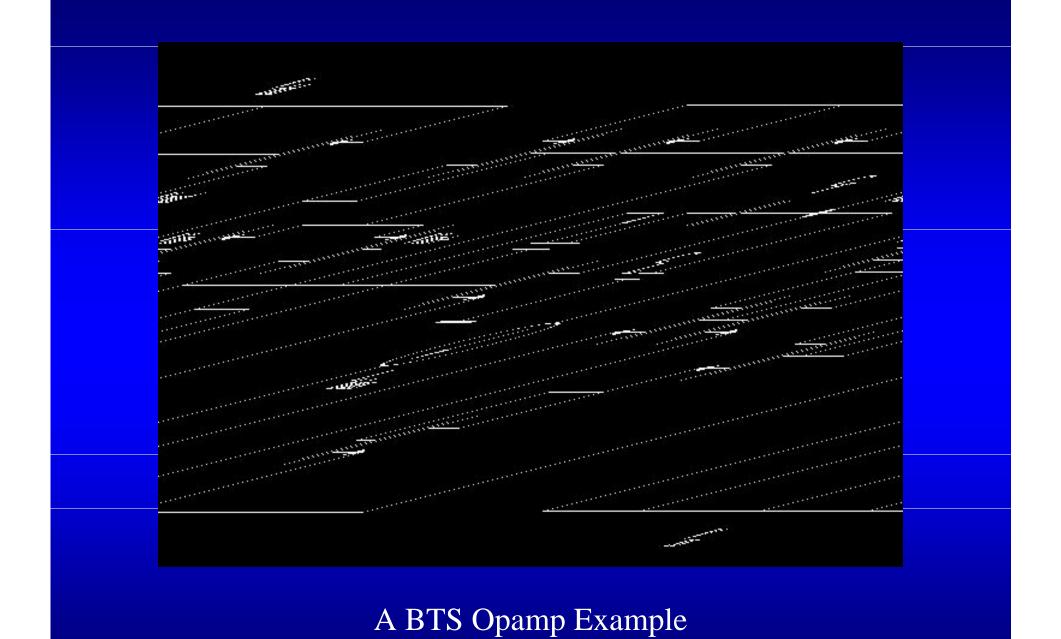


Variation in certain physical parameters (Tox, Nsub, Vth) with respect to wafer center creates a distribution of bias conditions across the wafer.

The effects of this distribution are incorporated into the optimization as a penalty term.

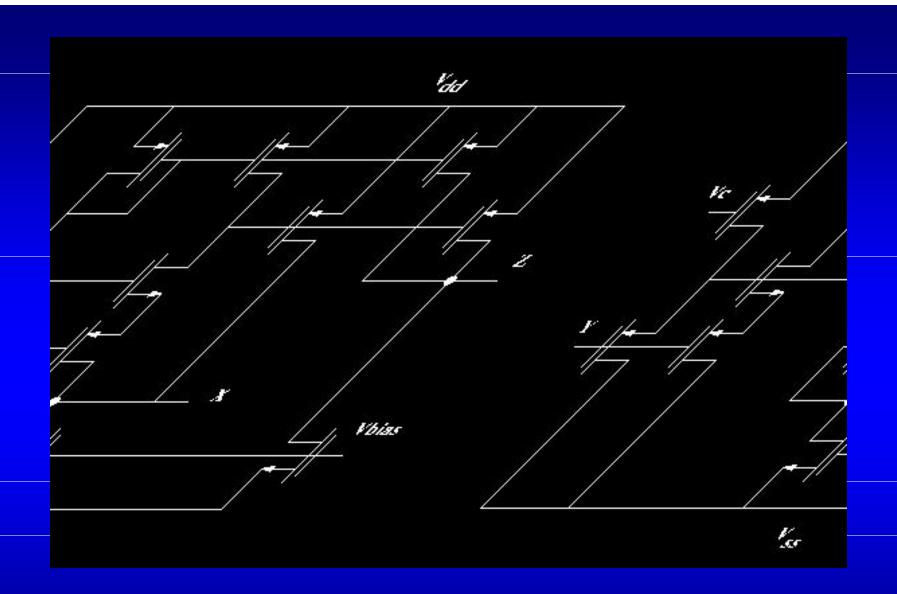
Wafer





## Results: Basic two Stage OPAMP

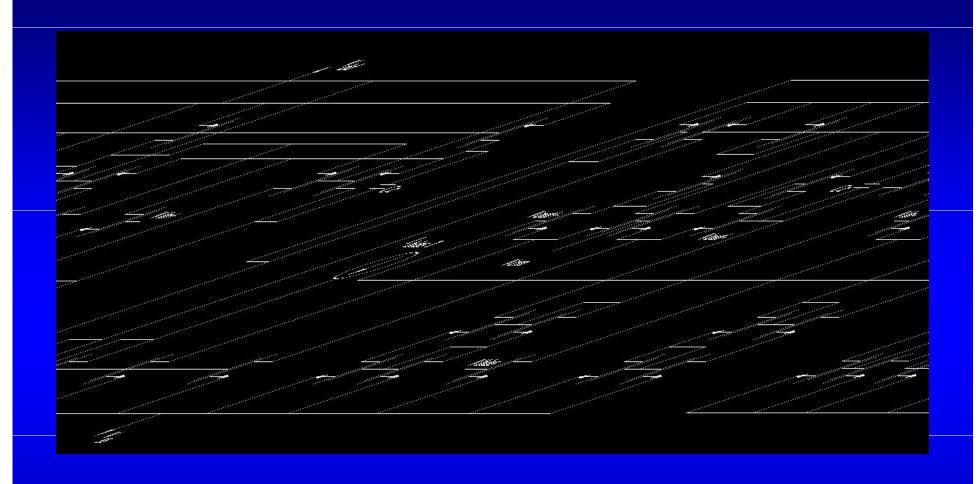
Attribute	Specification	Synthesis (HSPICE)
Capacitive load (pF)	1	1
Supply (V)	5	5
DC Gain (dB)	>75	81.5
Gain-BW (MHz)	>1	2.2
Phase Margin	>50	92.7
Slew rate (V/µs)	>0.53	1.62
Static Power (mW)	<10	0.378
Output Swing (V)	>3	4.96



A Current Conveyor Example

# Results: Current Conveyor

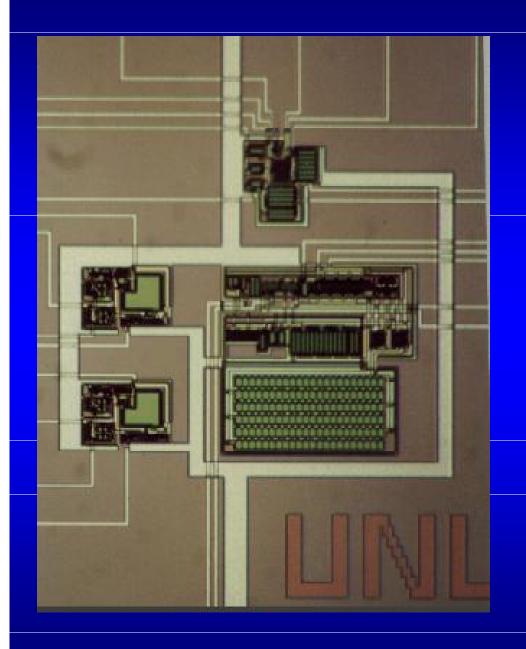
	Attribute	Specification	Synthesis (HSPICE)
	Supply (V)	+5, -5	+5, -5
	Static Power (mW)	<20	11.8
	XY Terminal average error (mV)	<10	6.2
	ZY Terminal average error (mV)	<10	6.2
	Bandwidth of Z terminal (MHz)	<100	78



A Fully-Differential Folded-Cascode Operational Amplifier

#### Results: Folded Cascode OPAMP

Attribute	Specification	Synthesis
Supply (V)	+5 ,-5	+5, -5
Static Power (mW)	<30	7.59
DC gain (dB)	>60	65.4
Gain x BW (MHz)	High	94
CMRR	>100	765
Phase Margin	>50	88
Output Impedance (kΩ)	>80	100
Offset Voltage (V)	>0.4	0.2
Output Swing (V)	>2	3.2



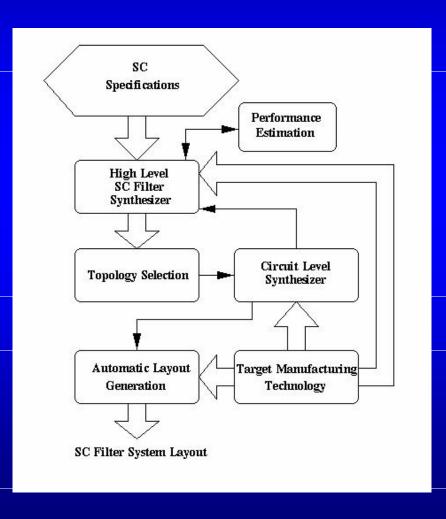
Prototype Test Chip Contains: BTS Opamps Current Conveyor Folded Cascode Opamp

Fabrication Technology: AMI – 1.5 micron Standard CMOS Process (2200 μm x 2200 μm)

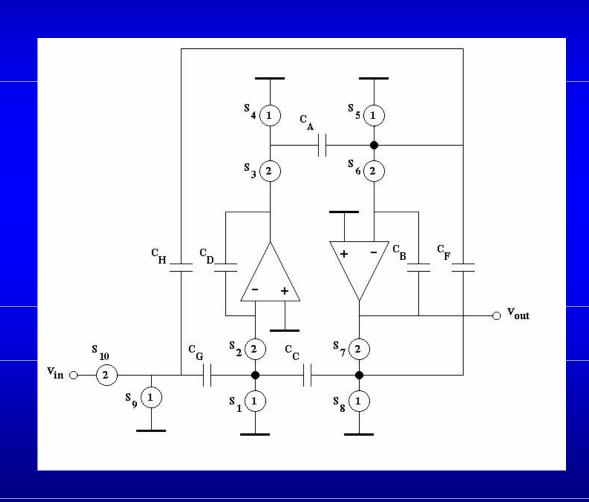
# Results: Verification on Silicon for BTS OPAMP (1.5 µm CMOS)

Attribute	Specification	Measured
DC Gain (dB)	>75	76 (81.5)
Gain x BW (MHz)	>1	1.13 (2.2)
Phase Margin	>50	84 (92.7)
Slew Rate (V/µs)	>0.53	0.64 (1.62)
Output Swing (V)	>3	4.6 (4.96)

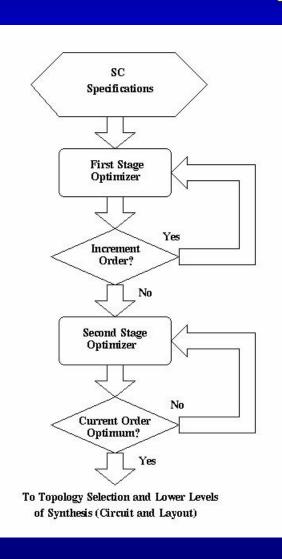
# Next Step: System Level Analog Synthesis (SC Filter Application Example)



# **Using Biquads**

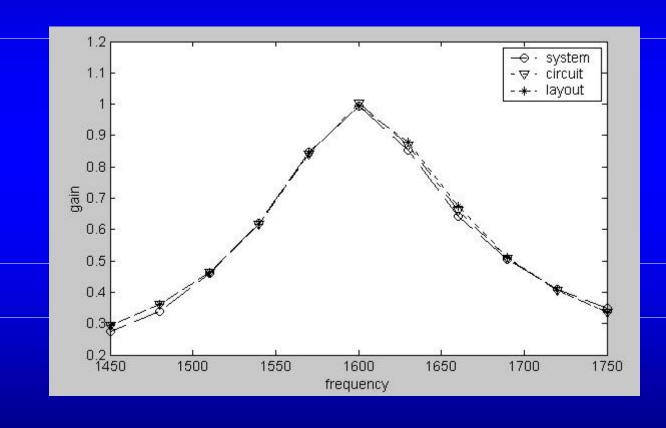


### High-Level SC Filter Synthesizer



#### A DTMF Filter Example

Q = 25 $f_{center} = 1600 \text{ Hz}$ 



#### **CONCLUSIONS**

- Presented a methodology for circuit-level analog
  CAD
- Validation on silicon
- Future Work: Development of System-level Automatic Synthesis tools (An initial attempt on SC Filter Synthesis is presented)
- Next crucial step: Analog VLSI applications